REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. Claims 2 and 32 have been cancelled. Claims 1, 3-5, 11, 14, 18, 21, 24-28, and 31 have been amended. Existing claims 1, 3-31, and 33 remain in the application.

ARGUMENT

Claim Rejections – 35 USC § 112

Claims 11, 14, 18, 21, 24, and 28 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

The Examiner rejected these independent method claims for the reason that the phrase "inner relationship" was not described in the specification as to enable one of ordinary skill in the art to make and/or use the invention. In response filed on April 20, 2006, Applicant presented arguments that this rejection should be withdrawn. In response, the Examiner rejected Applicant's arguments for two reasons: (1) evidence provided by Applicant is not sufficient to overcome the rejection for lack of enablement under 35 USC 112, first paragraph; (2) evidence to supplement a specification which on its face appears deficient under 35 USC § 112 must establish that the information which must be read into the specification to make it complete would have been known to those of ordinary skill in the art.

Here Applicant respectfully disagrees. First, the evidence provided by Applicant is sufficient to overcome the rejection for lack of enablement under 35 USC § 112, first

paragraph. The specification (see e.g., paragraph [0014] of the specification) along with the claim language in the initial disclosure makes the disclosure enabling for the limitation "inner relationship." The Examiner's main point is: were the description that an "inner cache" is referred to as an L1 cache and "outer cache" as an L2 cache considered as enabling for "inner relationship," the limitation "inner relationship" would be equivalent to "L1 relationship." Applicant respectfully disagrees with this argument presented by the Examiner. It is common known that caches are classified as L1, L2, or L3 based on their closeness to the processor. L1 cache is built into the processor and thus is normally referred to as "inner cache;" while L2 is normally external to a processor and thus is normally referred to as "outer cache." For reference only, the Examiner may look "L1 cache" or "L2 cache" in any technical dictionary (e.g., http://www.webopedia.com/"). Based on this fact, the "inner relationship" is relative to a processor. When claims 11, 14, 18, 21, 24, and 28 use the term "inner relationship," it implies that the first cache is closer to the processor than the second cache. Thus, the limitation "inner relationship" can be reasonably inferred from the specification and the evidence from the specification is sufficient to overcome the rejection for lack of enablement under 35 USC § 112, first paragraph.

Second, the evidence to supplement the specification (i.e., L1 cache is closer to the processor than L2 cache) is known to those of ordinary skill in the art as evidenced by the definition of L1 or L2 cache in a technical dictionary (e.g., http://www.webopedia.com/).

For the forgoing, Applicant strongly believe that the initial disclosure is enabling for the limitation "inner relationship" recited in claims 11, 14, 18, 21, 24, and 28. Thus,

Applicant respectfully requests that the Examiner reconsider Applicant's arguments and withdraw this rejection under 35 USC § 112, first paragraph.

Claim Rejections – 35 USC § 103

Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) (hereinafter Arimilli_1) in view of WO 00/52582 (hereinafter WO reference).

Claims 2-10 and 32-33 are rejected under 35 U.S. C. 103(a) as being unpatentable over Arimilli_1 in view of the WO reference and further in view of Arimilli (2002/0129211) (hereinafter Arimilli_2).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 706.02(j). Here the Examiner failed to establish a prima facie case of obviousness because at least the combination of Arimilli_1 and the WO reference does not teach or suggest all the claim limitations. For example, the combination of Arimilli_1 and the WO reference does not teach or suggest a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface. In the Final Office Action issued on July 19, 2006, the

Examiner asserted that the WO reference discloses this limitation. Applicant respectfully disagrees.

The Examiner specifically cited Fig. 1; page 11, lines 16-32; and page 12, lines 21-27 of the WO reference as disclosing the above-mentioned limitation. A careful review of the cited portion of the WO reference reveals that they do not disclose the claimed limitations. Although Fig. 1 of the WO reference shows that two coherency states may be associated with a cache line. However, the cited portion of the WO reference does not disclose that a first cache coherency state is associated with accesses from the first interface and a second cache coherency state is associated with accesses from the second interface. In fact the cited portions of the WO reference do not disclose how the two coherency state method as shown in Fig. 1 works. Because the cited portions of the WO reference do not teach or suggest the claimed limitation as recited in independent claims 1 and 31, the Examiner has not established a prima facie case of obviousness under 35 USC § 103. Thus, Applicant respectfully requests that the 35 USC § 103 rejections of independent claims 1 and 31 over Arimilli_1 in view of the WO reference be withdrawn.

Additionally, independent claims 1 and 31 have been amended to incorporate limitations from original claims 2 and 32, respectively. As a result, claims 2 and 32 have been cancelled. In rejecting original claims 2 and 32, the Examiner admitted that Arimilli_1 and the WO reference do not teach the first cache coherency state has higher privilege than the second cache coherency state when the second interface is coupled to a processor. However, the Examiner asserted that paragraphs [0002] and [0010] of Arimilli_2 disclose this limitation. Applicant respectfully disagrees.

Applicant argued in his response to the first Office Action issued on November 11, 2005 that the combination of Arimilli_1 and Arimilli_2 does not teach or suggest the limitation of **TWO** cache coherency states associated with one cache line, the first state when accessed from a first interface and the second state when accessed from a second interface. The Examiner accepted this argument by withdrawing original rejections and issuing new rejections based on the combination of Arimilli_1 and the WO reference. In fact, Arimilli_2 does not disclose this limitation (i.e., two cache coherency states associated with one cache line) at all. Without teaching or suggesting this limitation, it is impossible for Arimilli_2 to disclose that the first cache coherency state has higher privilege than the second cache coherency state when the second interface is coupled to a processor because a cache line must have two cache coherency states associated with it in order for the limitation recited in original claims 2 and 32 to make sense. The cited portions of Arimilli_2 (i.e., paragraphs [0002] and [0010] do not teach or suggest anything related to the limitation of two cache coherency states associated with one cache line. Without any hint from Arimilli_2 for the limitation of two cache coherency states associated with one cache line, it cannot be believed that a person of ordinary skill in the art can come up with the limitation recited in original claims 2 and 32 prior to the date the present application was filed. Thus, the combination of Arimilli_1 and Arimilli_2 does not teach or suggest the limitation recited in original claims 2 and 32, which is not taught or suggested by the WO reference either. This limitation is allowable over the combination of Arimilli_1, Arimilli_2, and the WO reference. By incorporating the limitation recited in original claims 2 and 32 to independent claims 1 and 31, respectively, independent claims 1 and 31, as amended,

are hence allowable over the combination of Arimilli_1, Arimilli_2, and the WO reference.

Because independent claims 1 and 31, as amended, are now patentable over Arimilli_1 in view of the WO reference further in view of Arimilli_2, all of the claims that depend therefrom (i.e., claims 3-10 and claim 33, respectively) are also patentable over the combination of Arimilli_1, Arimilli_2, and the WO reference.

Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli_2 in view of the WO reference.

Regarding independent claims 11, 14, 18, 21, 24, and 28, the Examiner asserted that Fig. 3, page 7; line 27 to page 8, line 13; and page 15, lines 1-19 of the WO reference discloses the limitation of transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces. Applicant respectfully disagrees. Fig. 2 of the WO references shows a state transition diagram based on MESI protocol and Fig. 3 of the WO reference shows the state transition diagram based on the MESI protocol with expanded coherency states (i.e., joint states). There is no showing by the cited portions of the WO reference of transitions from a single MESI coherency state (e.g., M or E) to a joint coherency state (e.g., MI), as recited by the claimed limitation.

In response to the above argument in the Advisory Action of October 16, 2006, the Examiner stated that the feature—transitions from a single cache coherency state (i.e., a single MESI state) to a joint coherency state (e.g., MI)—is not recited in the rejected claims. To make this feature more explicit in claims 11, 14, 18, 21, 24, and 28,

these claims have been amended to make it clear that the first cache coherency state is a single cache coherency state. By adding this limitation to claims 11, 14, 18, 21, 24, and 28, the limitation of transitioning the first cache coherency state to a joint cache coherency state, originally recited in these claims, is now very clear that it means transitions from a single state to a joint state.

For the foregoing reasons, the combination of Arimilli_2 and the WO reference does not teach or suggest all of the limitations recited in independent claims 11, 14, 18, 21, 24, and 28, as amended. Thus, these claims are patentable over Arimilli_2 in view of the WO reference. Accordingly, all of the claims that depend therefrom are also patentable over Arimilli_2 in view of the WO reference. Applicant hereby respectfully requests that the Examiner withdraw the 35 USC § 103 rejections of claims 11-30 and reconsider the application.

CONCLUSION

In view of the foregoing, existing claims 1, 3-31, and 3 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Early issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,

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